IN THE CLAIMS:

Please consider the following claims:

1. (currently amended) In a feedback equalizer device implementing a filter unit performing convolution operations between filter coefficients and one of a plurality of first discrete digital level values for generating a filter output, a multiplier device for multiplying a first discrete digital level value with a filter coefficient for said convolution operation, said multiplier device comprising:

a decoder device for receiving and decoding an encoded, first discrete digital level value to be multiplied with a filter coefficient, and implementing logic for generating control signals according to said first digital level value;

a first sub-multiplication circuit receiving said filter coefficient and implementing logic for multiplying said filter coefficient by ~~a positive value,~~ a negative value ~~or zero (0)~~ in accordance with a first set of control signals and generating a first intermediate multiplication result therefrom;

a second sub-multiplication circuit simultaneously receiving said first intermediate result and implementing logic for multiplying said first intermediate result ~~filter coefficient~~ by a positive value~~, a negative value~~ or zero (0) in accordance with a second set of control signals and generating a second intermediate result therefrom;

a third sub-multiplication circuit for shifting bits to effect a multiplication of one of said first or second intermediate result with a discrete digital value different than any of said first plurality of discrete digital level values, and generating a third intermediate result; and

an accumulator device for adding the results of said third and the other of said first or second intermediate results to obtain a final multiplication result.

2. (previously presented) The multiplier device as claimed in Claim 1, wherein said decision feedback equalizer is implemented in a communication system for processing signals in accordance with a ATSC (8-VSB) DTV standard, said plurality of first discrete digital level values including: +7/-7, +5/-5, +3/-3, and +1/-1 and represented as a three (3)-bit code signal.

3. (previously presented) The multiplier device as claimed in Claim 2, wherein said third sub-multiplication circuit shifts bits for a multiplication of one of said first or second intermediate result with a discrete digital value of four (4) or eight (8) in accordance with a third set of control signals.

4. (previously presented) The multiplier device as claimed in Claim 2, wherein said first and/or said second sub-multiplication circuit comprise an inverter circuit.

5. (previously presented) The multiplier device as claimed in Claim 2, wherein said multiplier device includes one or more inverter circuits implemented as an XOR circuit.

6. (original) The multiplier device as claimed in Claim 2, wherein said accumulator device comprises a carry save adder device for generating sum and carry results.

7. (original) The multiplier device as claimed in Claim 6, wherein said accumulator device further comprises a ripple adder device for adding said sum and carry results.

8. (original) The multiplier device as claimed in Claim 7, wherein said ripple adder device receives one or more said control signals for bit correcting bits when a multiplication by –1 is performed according to a first or second control signal step.

9. (previously presented) The multiplier device as claimed in Claim 6, further including a register for storing a filter result for use in said convolution operation, said accumulator device further adding a stored filter result with a final multiplication result of a current iteration.

10. (previously presented) The multiplier device as claimed in Claim 2, further including a device for encoding a first discrete digital level bit value as a set of bits.

11. (canceled).

12. (previously presented) A method for performing multiplication in a decision feedback equalizer device including a filter unit for performing convolution operations between filter coefficients and one of a plurality of first discrete digital level values, said method comprising:

a) decoding an encoded, first discrete digital level value to be multiplied by a filter coefficient, and implementing logic for generating control signals according to said first discrete digital level value;

b) performing two parallel operations, each operation including multiplying said filter coefficient by either +1 or -1 in accordance with said control signals for generating two intermediate results, and, corresponding operations for multiplying a corresponding intermediate result by +1 or zero (0) in accordance with said control signals and generating respective first and second intermediate results in parallel;

c) shifting bits to effect a multiplication of one of said first and second intermediate result with a second discrete digital value different than any of said plurality of first discrete digital level values, and generating a third intermediate result; and,

d) adding the results of said third intermediate result and the other of said first or second intermediate results to obtain a final multiplication result.

13. (previously presented) The method as claimed in Claim 12, wherein said decision feedback equalizer is implemented in a communication system for processing signals in accordance with a ATSC (8-VSB) DTV standard, said plurality of first discrete digital level values comprising: +7/-7, +5/-5, +3/-3, and +1/-1 and represented as a three (3)-bit code signal.

14. (previously presented) The method as claimed in Claim 13, wherein said shifting step c) includes the step of shifting bits to effect a multiplication of one of said first or second intermediate result with a discrete digital value of four (4) or eight (8) in accordance with said control signals.

15. (previously presented) The method as claimed in Claim 13, wherein said step of performing two parallel operations includes performing an inversion of said filter coefficient to be multiplied.

16. (canceled).

17. (previously presented) The method as claimed in Claim 13, further including the step of storing a filter result in a register for use during a corresponding operation in said filter unit, said adding step d) including adding said stored filter result with a final multiplication result of a current iteration to obtain a new filter value.

18. (previously presented) A multiplier device for multiplying one of a set of discrete digital level values with a filter coefficient comprising:

a decoder device for receiving and decoding an encoded, discrete digital level value to be multiplied and generating control signals according to said digital level value;

an inverter circuit providing two parallel operations, each operation including multiplying a number by either +1/-1 in accordance with said control signals for generating two intermediate results;

a multiplier circuit receiving said two intermediate results and providing respective parallel operations for multiplying a corresponding intermediate result of said inverter circuit by +1 or zero (0) in accordance with a control signals and generating respective further intermediate results;

a logic circuit for shifting bits of one further intermediate result to effect a multiplication of one of said further intermediate results with one of one or more discrete digital level values different than any of said discrete digital level values; and

an accumulator device for adding the results of said logic circuit shift multiplication with the other said further intermediate result to obtain a final multiplication result.

19. (previously presented) The multiplier device as claimed in Claim 18, for use in a filter device for performing a convolution operation in an adaptive feedback equalizer implemented in a communication system for processing signals in accordance with a ATSC (8-VSB) DTV standard, wherein said discrete digital level values include: +7/-7, +5/-5, +3/-3, and +1/-1, and said different discrete digital level values include four (4) and eight (8) in accordance with said control signals.